AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

1. (currently amended) A storage device comprising:

a nonvolatile memory; and

a control circuit,

wherein said nonvolatile memory has ~~a plurality of~~ a plurality of memory blocks, each of which has a plurality of sub memory blocks comprising a plurality of nonvolatile memory cells, and is capable of performing programming to a first sub memory block within a first memory block and a second sub memory block within a second memory block in parallel,

wherein said control circuit controls programming to said nonvolatile memory in accordance with ~~an~~ address information and data ~~in accordance with being~~ issued from an outside device,

wherein said first sub memory block of said first memory block includes a management area, which is used for storing [[a]] management information ~~which~~ and includes an area for storing [[a]] linking information between said first sub memory block of said first memory block and a corresponding sub memory block[[s]] of at least one other memory block[[s]],

wherein said control circuit ~~controls that~~ ~~reading~~ performs control to read said linking information from

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said first sub memory block of said first memory block in accordance with said address information, and ~~thereafter to~~ program~~programming~~ to ~~one or more of~~ said first sub memory block of said first memory block in accordance with said address information and to said corresponding sub memory block[[s]] ~~of other memory blocks relating to said first memory block by~~based on said linking information stored in said first sub memory block.

2. (currently amended) A storage device according to claim 1, further comprising a translation table,

wherein said translation table is used for translating from said address information issued from said outside device to a first physical address for selecting said first sub memory block of said first memory block, and

wherein said control circuit reads said linking information from said first sub memory block of said first memory block selected by said first physical address translated by said translation table from said address information.

3. (currently amended) A storage device according to claim 2, further comprising a buffer memory,

wherein said buffer memory is capable of storing data supplied from or ~~supplying~~ supplied to said outside device, and

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wherein said translation table is ~~storing~~ stored to said nonvolatile memory ~~when~~ before power supplying is turned off, and is ~~storing~~ stored to said buffer memory ~~when~~ after power supplying is turned on.

4. (currently amended) A storage device according to claim 3,

wherein said nonvolatile memory cells ~~including said~~in said first sub memory block[[s]] are coupled to a word line, and

wherein said selecting of said first sub memory block ~~is~~ includes selecting said word line corresponding to said physical address.

5. (currently amended) A storage device according to claim 4,

wherein when said control circuit detects ~~existing~~ an error in a nonvolatile memory cell in a ~~third~~ selected sub memory block ~~related~~ corresponding to ~~by said linking information in~~ said first sub memory block, said control circuit controls changing ~~said linking information replacing~~said selected sub memory block ~~said third sub memory block~~ to a ~~forth~~ different sub memory block in the same memory block and storing linking information of said different sub memory block into said first sub memory block.

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6. (currently amended) A storage device according to claim 5,

wherein in said programming to said first sub memory block, said control circuit controls reading data from said first sub memory block, merging data read from said first sub memory block and new data received from said outside device, and programming to a new first sub memory block[[,]] a second physical address [[of]] which is different from said first physical address of said first sub memory block.

7. (currently amended) A storage device according to claim 6,

wherein said control circuit controls changing said translation table ~~replacing~~ to replace said first physical address of said first sub memory block ~~to~~ by said second physical address of said new first sub memory block as a corresponding physical address of said address information received from said outside device, after programming to said new first sub memory block.

8. (currently amended) A storage device according to claim 7,

wherein said management information includes a first information which indicates, ~~that~~ for each of said first sub memory block and each said corresponding sub memory block[[s]] ~~of other memory blocks relating to said first memory block~~ by

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said linking information, whether the sub memory block is already erased or not.

9. (currently amended) A storage device according to claim 8, further comprising a plurality of volatile memories,

wherein each of said volatile memories is corresponding corresponds to each one of said memory blocks and is capable of storing program data.

10. (original) A storage device according to claim 9,

wherein in said programming to said first sub memory block, said control device controls reading data from said first sub memory block to said volatile memory corresponding to said first memory block.